## REMARKS

The Official Action mailed January 22, 2008, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant appreciates Primary Examiner Tran's time in conducting a telephonic interview on April 18, 2008. As described in more detail below, during the interview, agreement was reached as to the Examiner's request for additional information (pages 7-8, Paper No. 20080120). The Examiner agreed to waive the requirements of 37 CFR §§ 1.97 and 1.98 and enter the Information Disclosure Statement attached herewith, which constitutes a response to the Examiner's request for information (Id.).

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on March 18, 2004; and October 24, 2007.

Claims 1-31 are pending in the present application, of which claims 1-5, 7-9, 11-13 and 23-25 are independent. Claims 2-5, 8, 9, 12, 13 and 15-22 have been withdrawn from consideration by the Examiner (Box 4a, Office Action Summary; page 2, Paper No. 20080120). Accordingly, claims 1, 6, 7, 10, 11, 14 and 23-31 are currently elected, of which claims 1, 7, 11 and 23-25 are independent. Claims 1, 7, 11 and 23-25 have been amended to better recite the features of the present invention. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 6 of the Official Action rejects claims 1, 6, 7, 10, 11, 14 and 23-31 as anticipated by U.S. Patent No. 6,774,877 to Nishitoba. The Applicant respectfully traverses the rejection because the Official Action has not established an anticipation rejection.

As stated in MPEP § 2131, to establish an anticipation rejection, each and every element as set forth in the claim must be described either expressly or inherently in a

single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

The Applicant respectfully submits that an anticipation rejection cannot be maintained against the independent claims of the present application. Independent claims 1, 7, 11 and 23-25 already recite that a channel length of a first transistor is longer than a channel width thereof, and that a channel length of a second transistor is equal to or shorter than a channel width thereof. Also, dependent claims 6, 10 and 14 already recite wherein a ratio of the channel length to the channel width of the first transistor is equal to or more than 5. Further, independent claims 1, 7, 11 and 23-25 have been amended to recite that one of a source region and a drain region of a first transistor is connected to a light emitting element, that the other one of the source region and the drain region of the first transistor is connected to one of a source region and a drain region of a second transistor, and that a semiconductor layer of the first transistor continues to a semiconductor layer of the second transistor. The feature, that a semiconductor layer of the first transistor continues to a semiconductor layer of the second transistor, is supported in the present specification, for example, by Figure 5. For the reasons provided below, the Applicant respectfully submits that Nishitoba does not teach the above-referenced features of the present invention, either explicitly or inherently.

In the "Response to Arguments" section, the Official Action asserts that "Nishitoba et al. do teach the limitation 'that a channel length of a first transistor is longer than a channel width thereof'" (page 6, Paper No. 200980120). The Applicant respectfully disagrees and traverses the assertions in the Official Action.

The Official Action appears to misconstrue Nishitoba. Specifically, the Official Action appears to confuse disclosures in Nishitoba relating solely to the channel length and, in the Official Action, applies these disclosures relating to channel length to the channel width of transistors in the device. The actual disclosure of Nishitoba does not correspond to the assertions in the Official Action. The assertion in the Official Action,

i.e. "that a channel length of a first transistor is longer than a channel width thereof," is not supported in Nishitoba. Rather, Nishitoba merely appears to disclose the following (column 7, lines 42 to 58):

> ... The channel length of transistors 6 and 8 is 4 μm, and the channel width of transistors [7] to 9 is 4 μm ... the desired characteristics can be obtained by selecting the channel length of transistors 7 and 9 according to the picture quality that is demanded of the image display device ... The channel length of transistors 7 and 9 is preferably set to at least 0.5 times the channel length of transistors 6 and 8 ....

It appears that there is a typographical error at column 7, line 44, since it does not make sense to refer to the channel length of transistors "6 and 8" and compare them to the channel length of transistors "6 and 9." Based on the context of Nishitoba, it appears that column 7, line 44, should refer to "transistors 7 and 9" instead of "transistors 6 and 9," which is consistent with the rest of the paragraph. The reproduced portion of Nishitoba above has been corrected in a manner that is believed to be consistent with the context of Nishitoba. In any event, the assertions in the Official Action are not supported by the actual disclosure of Nishitoba.

The Applicant respectfully submits that one of ordinary skill in the art would recognize that Nishitoba merely teaches that the channel length of one set of transistors is the same as the channel width of another set of transistors, i.e. 4 μm. Also, Nishitoba appears to teach that the channel length of one set of transistors is preferably at least 0.5 times the channel length of another set of transistors.

However, Nishitoba simply fails to teach, either explicitly or inherently, that a channel length of a first transistor is longer than a channel width thereof, and that a channel length of a second transistor is equal to or shorter than a channel width thereof. Also, Nishitoba simply fails to teach, either explicitly or inherently, that a ratio of the channel length to a channel width of a first transistor is equal to or more than 5. Therefore, the Official Action has not set forth a proper anticipation rejection.

Furthermore, independent claims 1, 7, 11 and 23-25 have been amended to clarify that one of a source region and a drain region of a first transistor is connected to

a light emitting element, and that the other one of the source region and the drain region of the first transistor is connected to one of a source region and a drain region of a second transistor. Also, claims 1, 7, 11 and 23-25 have been amended to recite that a semiconductor layer of the first transistor continues to a semiconductor layer of the second transistor. The Applicant respectfully submits that one of ordinary skill in the art would understand that the latter feature means that the first transistor comprises a semiconductor layer, and that the second transistor comprises the same semiconductor layer. Alternately, one would understand that the latter feature means that the first transistor comprises a first region of a semiconductor layer, and that the second semiconductor layer comprises a second region of the same semiconductor layer. The Applicant respectfully submits that Nishitoba does not teach the above-referenced features, either explicitly or inherently.

Since Nishitoba does not teach all the elements of the independent claims, either explicitly or inherently, an anticipation rejection cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 102 are in order and respectfully requested.

Paragraph 9 of the Official Action requests the Applicant's assistance "in identifying all applications and/or patents that can be rejected under nonstatutory double patenting in regard to the instant application" (pages 7-8, Paper No. 20080120). The Applicant respectfully submits that this request goes well beyond the Applicant's duty of disclosure. Therefore, the Applicant contacted Primary Examiner Tran to clarify the request. During a telephonic interview conducted on April 18, 2008, agreement was reached as to the Examiner's request for additional information (Id.). The Examiner agreed to enter the Information Disclosure Statement, attached herewith, which constitutes the Applicant's response to the Examiner's request for information (Id.). Specifically, agreement was reached that it is appropriate for the Applicant to respond to the Examiner's request for information in the form of an Information Disclosure Statement and Form PTO-1449, and that it is not necessary to make any type of

statement or admission regarding double patenting. Also, noting the after final status of the present application, agreement was reached that the rules outlined in 37 CFR §§ 1.97 and 1.98 would be waived in this situation, and that the Examiner would enter the IDS without the normally requisite fee and certification due under Rules 97 and 98. As such, in presenting the IDS attached herewith, the Applicant has proceeded in accordance with the agreement reached with the Examiner on April 18, 2008. No further action is believed to be necessary to comply with the Examiner's request. The Examiner is thanked for her assistance in this regard.

Paragraph 10 of the Official Action provisionally rejects claims 23 and 24 under the doctrine of obviousness-type double patenting over claims 3, 4, 7, 8, 11, 12, 15 and 16 of Application Serial No. 11/208,278. As is discussed in greater detail above, the independent claims have been amended to better recite the features of the present invention. In light of this amendment, the Applicant respectfully traverses this ground for rejection and reconsideration of the pending claims is respectfully requested. In any event, the Applicant respectfully requests that the double patenting rejections be suspended until an indication of allowable subject matter is made in the present application. At such time, the Applicant will respond to any remaining double patenting rejections.

Paragraph 13 of the Official Action rejects claims 1, 6, 7, 10, 11, 14 and 23-31 under 35 U.S.C. § 112, first paragraph. Regarding claims 1, 7, 11 and 23-25, the Official Action asserts that the specification lacks support for "a first electrode of the first transistor is connected to the light emitting element" and for "a second electrode of the first transistor is connected to the second transistor" (pages 10-12, Paper No. 20080120). Regarding dependent claims 26-31, the Official Action asserts that the specification lacks support for "a first electrode of the third transistor is electrically connected to a signal line and a second electrode of the third transistor is electrically connected to the gate electrodes of the first transistor and the second transistor" (pages 12-13, Id.). Paragraph 15 of the Official Action rejects claims 1, 6, 7, 10, 11, 14 and 23-

31 under 35 U.S.C. §112, second paragraph, asserting that "the limitation of 'a second electrode of the first transistor is connected to the second transistor' is vague and indefinite because it is unclear if the 'second electrode' is synonymous with the instant claimed gate electrode" (pages 13-14, Id.). The Applicant respectfully disagrees and traverses the assertions in the Official Action.

The Official Action appears to express a concern that the claimed features are too broadly worded. However, broad terminology is acceptable so long as it is supported and definite. Specifically, the Applicant respectfully submits that Figure 2 clearly discloses a circuit configuration that corresponds to the claimed features and that one of ordinary skill in the art would clearly recognize from at least Figure 2 that the Applicant was in possession of the claimed invention at the time the application was filed. In this regard, it is not required that the claims find literal support in the specification, see MPEP 2163, stating "there is no *in haec verba* requirement," i.e., no requirement that the same terms be used in order for the disclosure to satisfy the description requirement.

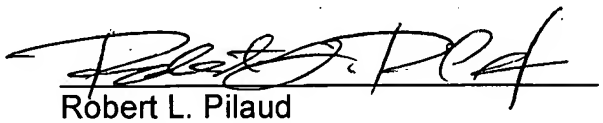
Also, it is noted that a "first electrode" and a "second electrode" may refer to source and drain electrodes of a transistor.

In any event, the Applicant has amended the independent claims for clarity. Specifically, the claims have been amended to recite that one of a source region and a drain region of a first transistor is connected to a light emitting element, and that the other one of the source region and the drain region of the first transistor is connected to one of a source region and a drain region of a second transistor.

The Applicant respectfully submits that the amended claims, when read in light of the specification, are adequately described and supported in the specification and definite. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 112 are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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